High performance voltage follower with very low output resistance for WTA applications

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Abstract: A modification of the conventional Flipped Voltage Follower (FVF) to enhance its output resistance is presented. It consists of replacing the conventional cascoding transistor of the basic cell by a regulated cascode scheme. This decreases the output resistance by a factor $g_m r_o$ approximately, the gain of a transistor as an amplifying stage. This is achieved with only two additional transistors and a biasing current I_B, offering a significant advantage with respect to other previously reported architectures that require considerably increased power consumption and number of devices. Simulation results in 0.5µm technology show an enhancement factor of 16, approximately, with respect to the conventional FVF, resulting in an output resistance of 3.1 Ω. Additionally, the proposed follower was implemented in a winner-take-all circuit to prove its functionality; simulation and experimental results confirm the proposed operation.

Keywords: analog CMOS integrated circuits, voltage follower, winner-take-all (WTA) analog circuits.

Classification: Analog CMOS integrated circuits

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1. Introduction

Portability of certain electronic devices has had a strong impact the past few decades, and the increasing competition from industry in this field has resulted in an evident demand for better performance, leading to innovative ideas for enhanced operation and reduced power consumption. Buffers, commonly used to drive demanding loads, have had the tendency to be designed with higher linearity, lower power consumption for increased efficiency, and ability to provide large output currents. An evident example of this is the denominated Flipped Voltage Follower (FVF) [1], shown in Fig. 1a. Designers have found variations for this high performance voltage follower in order to achieve increased linearity and frequency of operation [2]. It has also been subject of many applications such as highly linear differential amplifiers [3], and winner-take-all configurations (WTA) [4], where these implementations have demonstrated significantly enhanced performance compared to their equivalent conventional structures.

2. Conventional topologies of FVF

The conventional FVF shown in Fig. 1a is formed by two transistors and a current source I_B. Observe that M2 has a constant biasing current, inducing a constant gate-source voltage; therefore voltage variations at the input V_i are reflected at the output node V_o level shifted by the gate-source voltage of M2 V_{GS2}, thus resulting in $V_o = V_i - V_{GS2}$. Additionally, the shunt feedback provides the ability to adjust the voltage V_{GS1}, which allows M1 to sink large currents. Variations in V_{GS1} are attenuated by M2 by a factor $g_{m2}r_{o2}$ at the output node, where g_{m2} and r_{o2} are the transconductance gain and the drain resistance of M2 respectively. Hence, it offers a low output resistance of $R_o = 1/g_{m1}g_{m2}r_{o2}$ approximately.

Many approaches on how to enhance the output resistance have been proposed

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over the past few years. A common example is shown in Fig. 1b, reported by Shukla, et al. in [5] and by Retdian, et al. in [6], among others; this topology is based on feeding the output signal back to the input terminal by means of an amplifying stage, where a conventional op-amp or an operational transconductance amplifier (OTA) are typically used. Straight forward analysis shows that this inclusion enhances the output resistance by the open-loop gain of the amplifier, thus resulting in $R_o = 1/A_v^{OL} g_{m1} g_{m2} r_{o2}$, where A_v^{OL} is the open-loop gain of the amplifier. The amplifier in [5] consists on a simple differential pair with an open-loop gain of the form $g_m r_o$, consuming a current of $2I_B$ with a total of 6 devices. The amplifier in [6] consists on a differential amplifier with an open-loop gain of the form $Kg_m r_o$, where K is a multiplication factor based on an internal current scaling; although this represents an increase in current consumption and number of devices of $(2+K)I_B$ and 4+2K respectively.

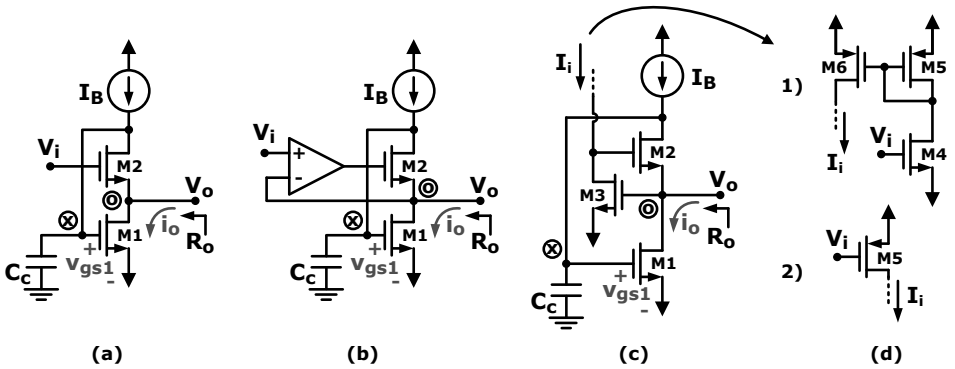

Fig. 1. a) Conventional Flipped Voltage Follower (FVF) [1], b) FVF with input op-amp to enhancement the output resistance [5], [6], c) Proposed FVF circuit including a regulated cascode stage, and d) examples of transconductors to provide the input current I_i from an input voltage V_i.

3. Proposed structure for output resistance enhancement

Note that the conventional FVF is similar to the input stage of a low-voltage cascoded current mirror [7], where M1 is the current sensing device and M2 is the cascoding transistor that attenuates gate-source voltage variations of M1. The latter, as previously discussed, has proved to lower the output resistance in the case of the FVF; hence, if this conventional cascoding technique is replaced with a regulated cascode scheme the output resistance can be reduced significantly. Fig. 1c shows this implementation where transistors M2 and M3 form the regulated cascode structure. In a conventional regulated cascode scheme, M3 is biased with a constant current; however, as the output voltage in the proposed circuit is defined by the gate-source voltage of this transistor, V_{GS3}, a current I_i is used as input to define it, and hence, the output voltage, which allows the possibility to use the circuit as a current-to-voltage converter. Also, structures for V-I current conversion (transconductors) can be employed at the input in order to operate the circuit as a high performance voltage follower. Examples of transconductors are shown in Fig. 1d; option 1 offers the same output dc level as the input, whereas

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option 2) exhibits signal inversion, hence permitting the circuit to act as an inverter. Additionally, the output voltage can also be controlled by defining a biasing current for M3 and using its source terminal as input, thus operating in common-gate configuration with an input resistance of $1/g_{m3}$, which becomes helpful for applications that require impedance matching such as RF receivers. The output node presents a very low resistance defined as:

$$R_o \approx \frac{1}{g_{m1}g_{m2}r_{o2}g_{m3}r_{o3}} \tag{1}$$

Which compared to the conventional FVF in Fig. 1a it shows an enhancing factor of $g_{m3}r_{o3}$ introduced by the regulated cascoded which, in 0.5µm technology, ranges from tens to a few hundreds. This enhancing factor of the form $g_m r_o$ is similar to the approaches reported in [6] and [7]. However, in the proposed structure this is achieved with only two additional devices (or four in the case of the inverter) and an input current; contrary to the case of [6] that requires an additional current of 2IB and six extra transistors, as well as to the one in [7] which requires an additional current of $(2+K)I_B$ and 4+2K transistors.

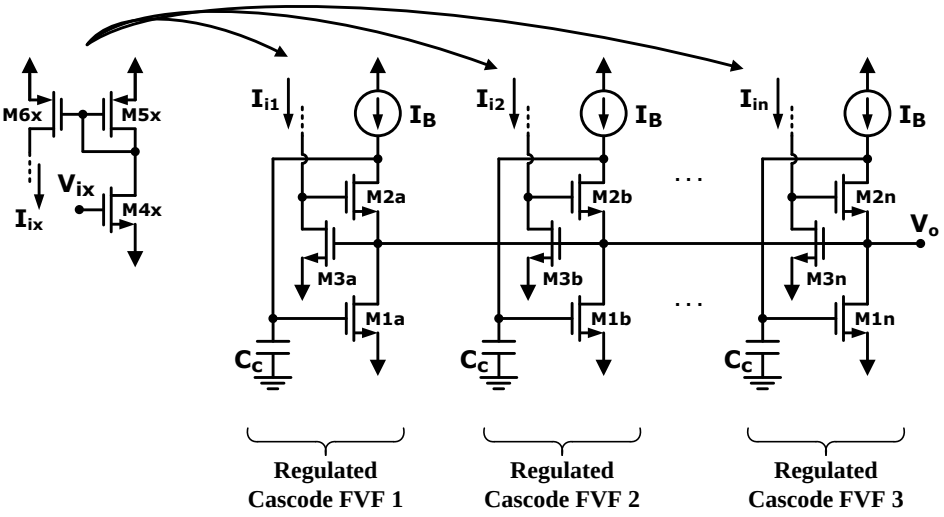

Fig. 2 Implementation of a WTA using the proposed circuit.

Similar to the conventional structures in Fig. 1a and 1b, the negative shunt feedback of the proposed circuit suggests frequency stability to be studied. Small-signal analysis following the same methodology as in [1], shows that the first non-dominant pole is located at the output node defined as $\omega_{po} \approx g_{m1}g_{m2}r_{o2}g_{m3}r_{o3}/C_L$, where C_L is the loading capacitance. The gain bandwidth product is defined as $GB = g_{m1}/C_c$; hence, following a commonly used condition to ensure stability given by $2GB < \omega_{px}$ we find an expression for the compensating capacitor as $C_c > 2C_L/g_{m2}r_{o2}g_{m3}r_{o3}$. Also, note that when using the circuit as a voltage follower with either of the options in Fig. 1d, the operational output range is defined by the expression $V_{DD} - V_{SS} - V_{TH3} - V_{GS2} - V_{DS5}^{sat}$.

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4. Design of a WTA using the proposed voltage follower

Winner-take-all (WTA) circuits perform fundamental operations (minimum/maximum voltage for several input signals) for many non-linear signal processing applications, and are based on the common-source configuration of a transistor. The proposed follower was implemented in the WTA circuit shown in Fig. 2, similarly to that reported in [4], to test its operation. It consists of *n* identical sub circuits connected to a low-resistive node. The cell with the lowest input voltage is capable to maintain its corresponding transistor M2i (for i=1, 2, …n) in saturation, thus controlling the output voltage; in the case of the remaining cells M2i enters in deep triode region, hence loosing low output resistance of the cell and capability to follow an input signal.

5. Simulation and experimental results

The proposed circuit and WTA were simulated in 0.5µm CMOS technology using spectre. The nominal threshold voltages are V_{THN} = 0.7 V, V_{THP} = -0.9 V for NMOS and PMOS respectively, and sizes 12/1.2 µm/µm and 36/1.2 µm/µm for NMOS and PMOS transistors respectively. The circuits were tested with a supply voltages V_{DD}= -V_{SS} = 1.5 V, a biasing current I_B = 100 µA, and C_c = 3pF in all cases.

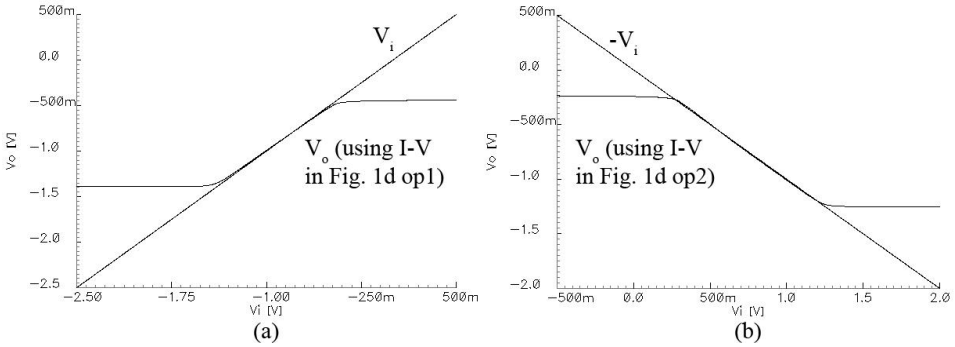

Fig. 3 DC transfer characteristic of the proposed circuit using the V-I converter (transconductor) in a) Fig. 1d option 1 and b) option 2.

Fig. 3a shows the dc transfer characteristic of the proposed circuit when used as a voltage follower, implemented with the transconductor in Fig. 1d option 1). Fig. 3b shows the transfer characteristic of the proposed circuit when used as an inverter, implemented with the transconductor in Fig. 1d option 2).

Additionally, a prototype using commercial transistor arrays ALD06-07 was assambled (NMOS and PMOS respectively). Their parameters are: $\beta = \mu C_{ox}(W/L) = 480\ \mu A/V^2|_{NMOS}$, $220\ \mu A/V^2|_{PMOS}$, $\lambda = 0.05\ V^{-1}|_{NMOS,PMOS}$, $|V_T| = 0.7\ V|_{NMOS,PMOS}$, and $\gamma = 0.3\ \sqrt{V}$. The circuits were tested with supply voltages of V_{DD}= -V_{SS} = 2 V, and a biasing current I_B = 50 µA.

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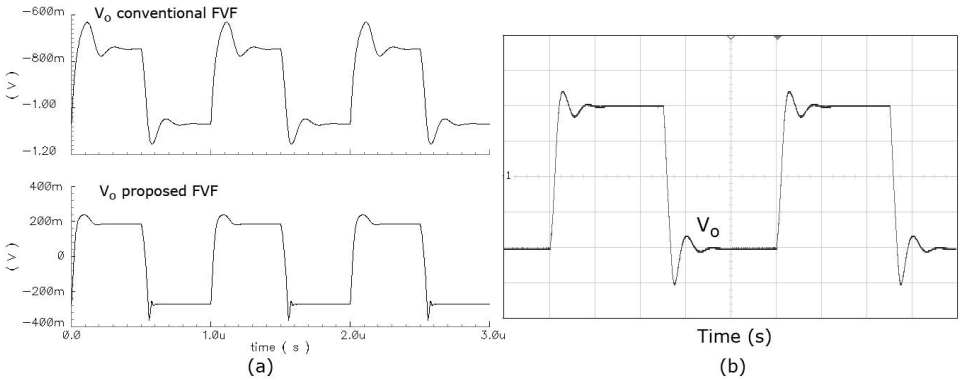

Fig. 4 a) Simulated transient response of the conventional FVF in [1] and the proposed circuit for a square input signal of V_i=0.4V_{pp} at 1MHz driving a loading capacitor of C_L=15pF; and b) experimental response of the proposed circuit for an input signal of V_i=0.4V_{pp} at 100kHz with C_L = 55pF (*x* axes is 2µsec/□, and *y* axes is 100mV/□).

Fig. 4a shows the simulated transient response of the conventional FVF in [1] and the proposed circuit in Fig. 1c for an input signal of V_i = 0.4V_{pp} at 1MHz. The conventional FVF offers a slew rate of SR+/-=10.3 / 10.5 V/µsec, whereas the proposed circuit has SR+/- =14.2 / 13.08 V/µsec, with a loading capacitor of C_L = 5 pF, resulting in an enhancing factor of ~1.4. Fig. 4b shows the experimental output voltage of the proposed circuit for an input signal of V_i = 0.4V_{pp} at 100kHz, offering slew rates of SR+ = 2.5 V/µs and SR- = 2.67 V/µs with a loading capacitor of C_L = 55 pF. Table 1 shows a comparison between simulated parameters of the conventional and proposed structures, where the proposed structure shows an advantage in terms of power consumption and silicon area. Fig. 5a shows the simulated transient response of the implemented WTA using the proposed follower for *n*=3. The three input signals are a sine wave form V_{i1}=0.4V_{pp} at 100kHz, a triangular form V_{i2}=0.4V_{pp} at 50kHz, and a dc level of V_{i3}=0V. Fig. 5b shows the experimental result for input signals of a triangular form V_{i1}=0.4V_{pp} at 4kHz, a sine wave form V_{i2}=0.5V_{pp} at 1kHz, and a dc level of V_{i3}=0V.

Table I. Simulated parameters of the proposed circuit and conventional voltage followers.

Measured parameter	Variation of FVF in [5]	Variation of FVF in [6] (K=10)	This work (Fig. 1c)
R_o [Ω]	2.8	1.2 -> 5	3.1
R_o enhancing factor	$g_m r_o$	$Kg_m r_o$	$g_m r_o$
Minimum supply V	$V_{GSN}+3V_{DS}^{sat}$	$V_{SGP}+2V_{DS}^{sat}$	$2V_{GSN}+V_{DS}^{sat}$
Power dissipation	900 µW	3900 µW	~600 µW
Silicon area	1833 µm^2	4386.37 µm^2	1018 µm^2

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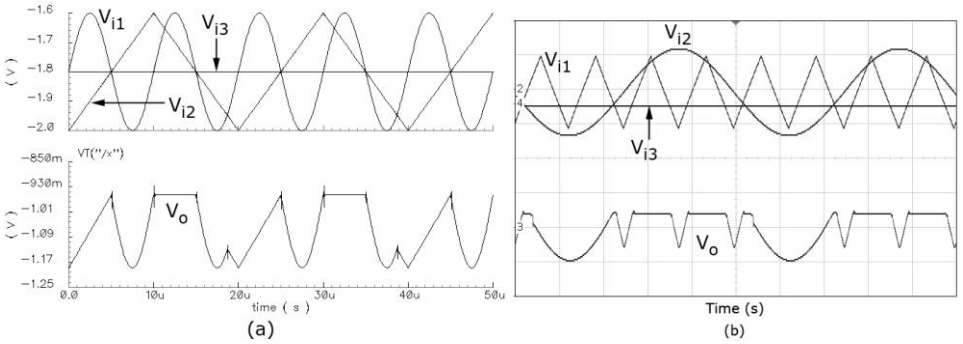

Fig. 5 a) Simulated transient response of the WTA implemented with the proposed circuit for input signals: a sine wave V_{i1}=0.4V_{pp} at 1kHz, a triangular form V_{i2}=0.4V_{pp} at 500Hz, and a dc level of V_{i3}=0V; and b) Experimental response for input signals of a triangular form V_{i1}=0.4V_{pp} at 4kHz, a sine wave form V_{i2}=0.5V_{pp} at 1kHz, and a dc level of V_{i3}=0V (axis: *x* is 200μsec/□, *y* is 200mV/□).

5. Conclusion

A variation of the conventional Flipped Voltage Follower (FVF) to improve the output resistance was discussed. Basing the implementation in a regulated cascode scheme only two additional transistors and an input current are required. Analytically, the proposed scheme reduces the output resistance by a factor $g_m r_o$, resulting in a very-low resistive node of 3.1Ω. The operation was confirmed by implementing the proposed follower in a winner-take-all circuit; simulation results demonstrate the operation of the implementation.

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